TECHNICAL REPORT: PHYSICAL ELECTRONICS

A MAGNETIC REVERSIBLE COUNTER WITH DIGITAL-TO-ANALOG CONVERSION

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WORK CARRIED OUT AS PART OF THE LOCKHEED INDEPENDENT RESEARCH PROGRAM.

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A MAGNETIC REVERSIBLE COUNTER WITH DIGITAL-TO-ANALOG CONVERSION

by

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WORK CARRIED OUT AS PART OF THE LOCKHEED INDEPENDENT RESEARCH PROGRAM

Lockheed

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SUNNYVALE, CALIFORNIA

FOREWORD

This report describes the operation of the Magnetic Reversible Counter with Digital-to-Analog Conversion. The counter is significantly improved by the use of magnetic circuits instead of semiconductors. The improvement consists of reduction in parts count with attendant increase in reliability. Although magnetic circuits have been discussed in the literature, it is difficult to find a system in which the special characteristics of these circuits have been used to advantage.

Acknowledgments are expressed to: C. G. LeVezu, for many helpful suggestions; N. B. Dean, for invaluable assistance in building and checking out the system; and M. Blumberg and R. Lucero, for assistance and suggestions in drafting the manuscript.

ABSTRACT

This report describes a time-shared, two-channel magnetic counter and digital-to-analog converter. The counter is capable of performing unit addition and subtraction. The design objective – to reduce the number of components – was well satisfied by the use of all-magnetic shift registers as the storage elements. Only two components are required for magnetic storage, whereas ten components were required for transistor flip-flop storage.

The logic operations were performed by time-shared diode gate circuits. The calculated worst-case error for the digital-to-analog conversion is ±0.3 percent. The measured error is less than ±0.25 percent. This error is due to variations in the bulk resistivity of diodes and PNPN switches, and it can be reduced, theoretically, to less than ±0.1 percent.

CONTENTS

ILLUSTRATIONS

Section 1
INTRODUCTION

1.1 BACKGROUND

The system designed is an incremental digital-to-analog counter designed for use in an advanced missile flight-control system. The equipment has two time-shared channels capable of performing addition or subtraction by unity. The system was designed to reduce the number of components used in a previous design. Reduction was accomplished by replacing conventional semiconductor flip-flops with all-magnetic shift-registers.

An initial three-month effort was devoted to the design of an all-magnetic system. However, many problems arose that count not be solved within this time limit. Consequently, a hybrid system evolved, using magnetic cores and wire for the shift-register storage elements and semiconductors in the problem areas. Subsequent evaluation of the hybrid system revealed that the design objective for fewer components had been met. The component count was reduced by 22.9 percent with an attendant increase in reliability.

In addition to reduced component count, a system accuracy of ±0.1 percent without component selection was a development objective. Preliminary efforts in the digital-to-analog conversion were directed toward the use of a current switch. However, analysis showed that this approach, used in a previous system, yielded a system accuracy no better than 1.4 percent. The current switch was next replaced by a voltage switch. This resulted in a superior performance, giving a worst-case system accuracy of ±0.3 percent. Although not meeting the design objective of ±0.1 percent accuracy, the accuracy obtained was a fourfold improvement over the system which used current switches (Ref. 1).

1.2 REPORT OBJECTIVES

This report fulfills three objectives:

(1) To provide the final report on the Magnetic Reversible Counter with Digital-to-Analog Conversion, for an advanced missile flight-control system, developed by the Ground Digital Equipment organization

(2) To show how magnetic elements are applied to improve system performance

(3) To describe an ac digital-to-analog converter of a non-conventional design

The text is divided into three parts:

(1) Description of the circuits used, with an explanation of the principles of operation

(2) Error analysis of the digital-to-analog converter

(3) Detailed description of the system operation

Section 2
CIRCUIT DESCRIPTION

2.1 INTRODUCTION

The eleven different circuits used in the system are described in this section. Four of these circuits, the all-magnetic shift-register, blocking oscillator, 10-count magnetic scaler, and internal clock, make use of magnetic cores having square-loop hysteresis loops. These four, together with the other seven conventional circuits, are listed below:

- All-magnetic shift-register
- Blocking oscillator
- Clock and prime driver
- Voltage switch
- Ladder-adder
- 10-count magnetic scaler
- Internal clock
- OR gate
- AND gate
- Differentiating gate
- Flip-flop

2.2 ALL-MAGNETIC SHIFT-REGISTER

The all-magnetic shift-registers (Ref. 2) each consist of twenty multi-aperture ferrite cores interconnected with copper wire. There are two cores for each bit of the word, as shown in Fig. 2-1. Odd numbered cores are represented by O_1, O_2, etc., and even numbered cores by E_1, E_2, etc. As noted on Fig. 2-1, O_i, and E_i represent cores O_2 through O_9 and E_2 through E_9, respectively. Thus, each shift-register accommodates a ten-bit binary word. The timing cycle of events is shown in Fig. 2-2.

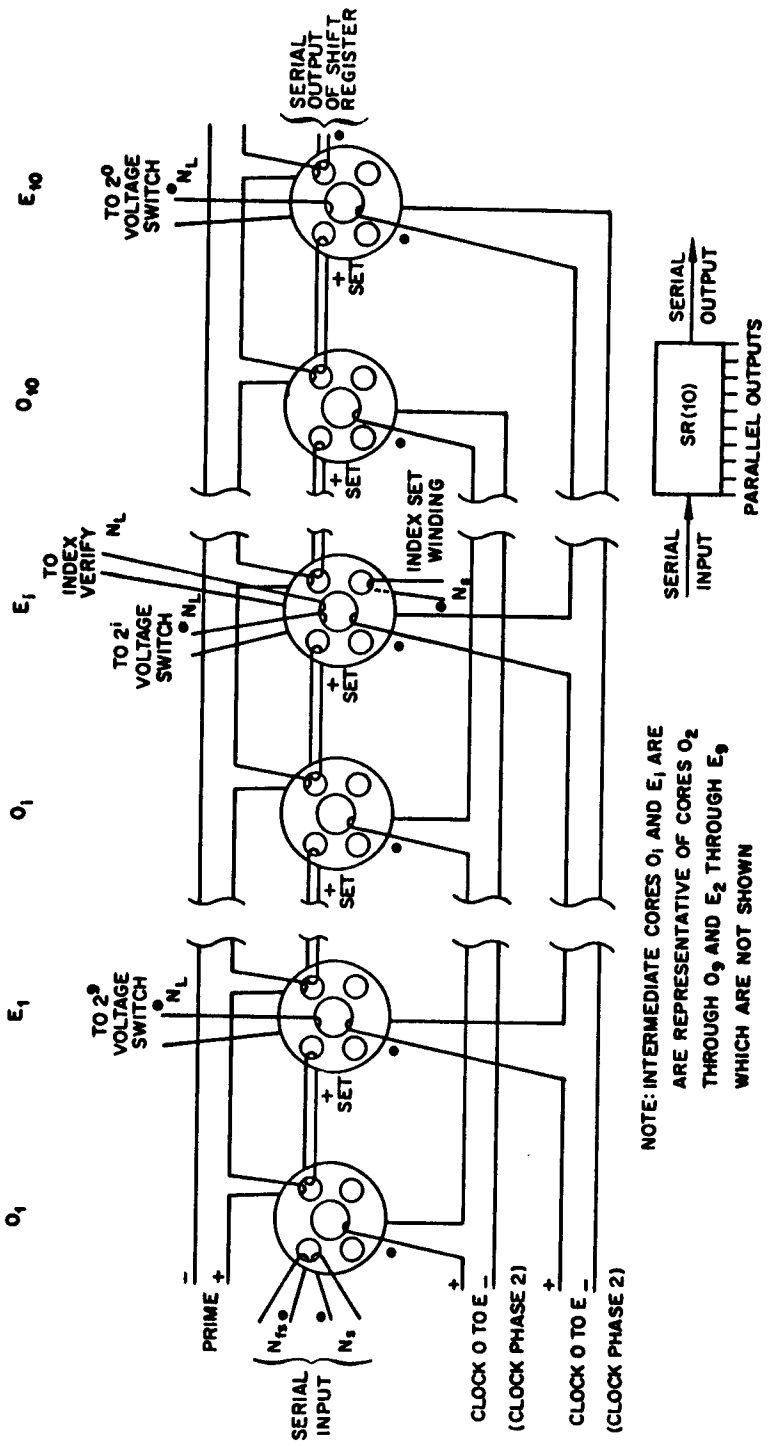


Fig. 2-1 All-Magnetic Shift-Register Schematic Diagram

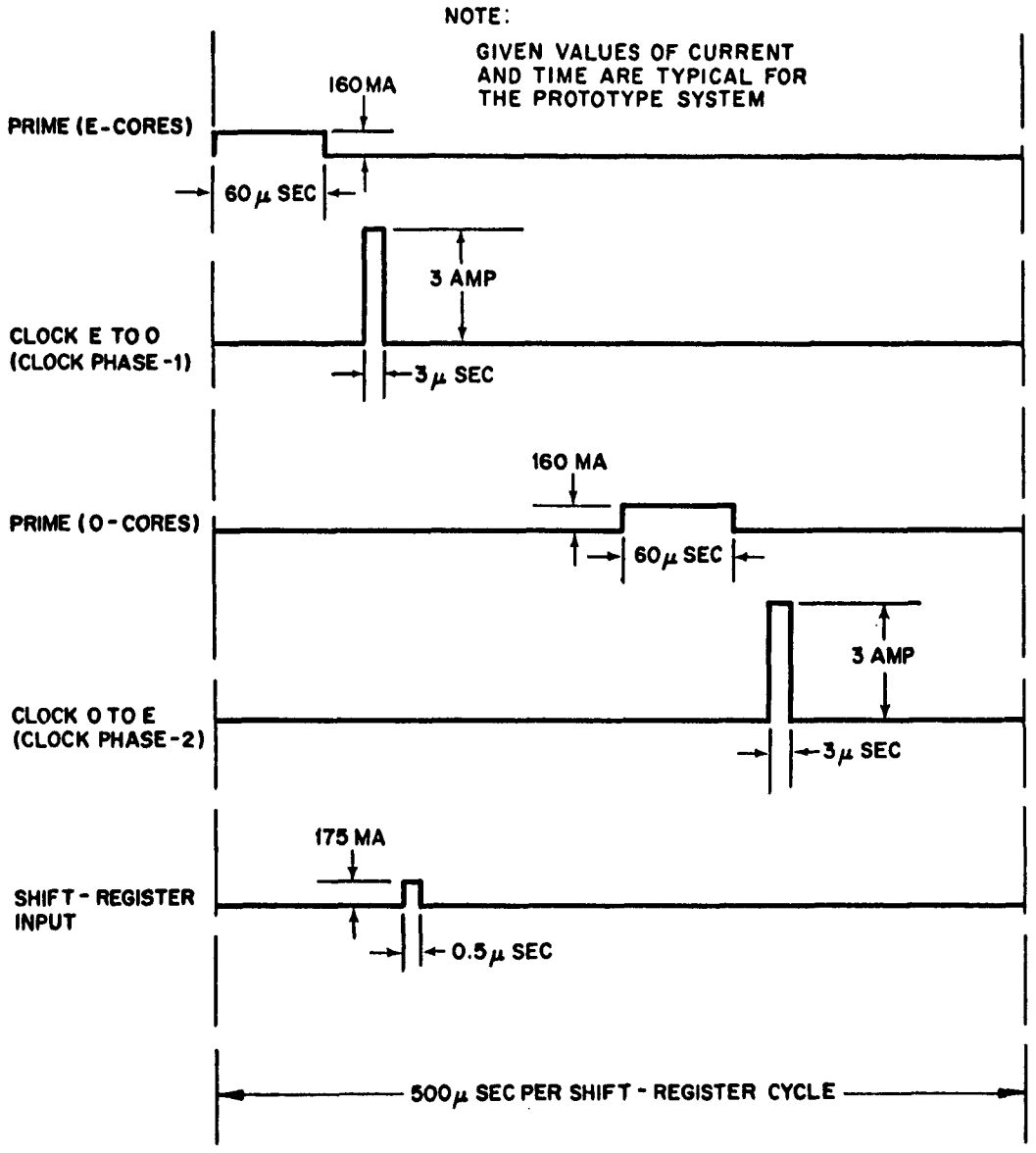


Fig. 2-2 Timing Cycle for All-Magnetic Shift-Registers

The circuit operation proceeds in the following manner. Assume that the core E_i, Fig. 2-1, has been set. The magnetic field within the core (Ref. 3) is shown in Fig. 2-3a. A prime pulse of current – typically 20 to 80 μsec in length and 125 to 300 ma in amplitude – is then applied, which changes the field pattern shown in Fig. 2-3a to that shown in Fig. 2-3b. The core is then reset (Fig. 2-3c) by the clock E to O current pulse which is, typically, 1 to 3 μsec in length and 2 to 5 amperes in amplitude. The field reversal due to this pulse causes a voltage to be induced in the winding linking core E_i and the adjacent core O_{i+1} and results in setting the O_{i+1} core. The same sequence of events is now applied to the O_{i+1} core. A prime core is followed by the clock pulse, designated O to E, which transfers the information into the core E_{i+1}. In the above manner, information is shifted through the register, from O_1 to E_1, E_1 to O_2, ..., O_i to E_i, E_i to O_{i+1}, ..., O_{10} to E_{10}.

2.3 BLOCKING OSCILLATOR

The input circuit for the shift-register is a blocking oscillator which sets the first odd core, O_1, of the shift-register. A positive signal applied to the base of transistor Q1, Fig. 2-4, saturates the transistor and causes a magnetizing current to flow in winding N_S of core O_1. This current tends to change the magnetic field in this core from that shown in Fig. 2-3c (reset state) to the pattern appearing Fig. 2-3a (set state). A portion of the voltage E_S developed during this field reversal, $N_{fb}/N_S \times E_S$, is fed back to the base of Q1, holding it on. This regenerative action ceases when the core is fully set because there is no longer a changing magnetic field available to sustain a voltage.

2.4 CLOCK AND PRIME DRIVER

The clock and prime driver (Ref. 4) develops both the clock pulses used to shift information in the all-magnetic shift-registers and the priming pulses in accordance with the timing relationships of Fig. 2-2. The circuit schematic appears in Fig. 2-5.

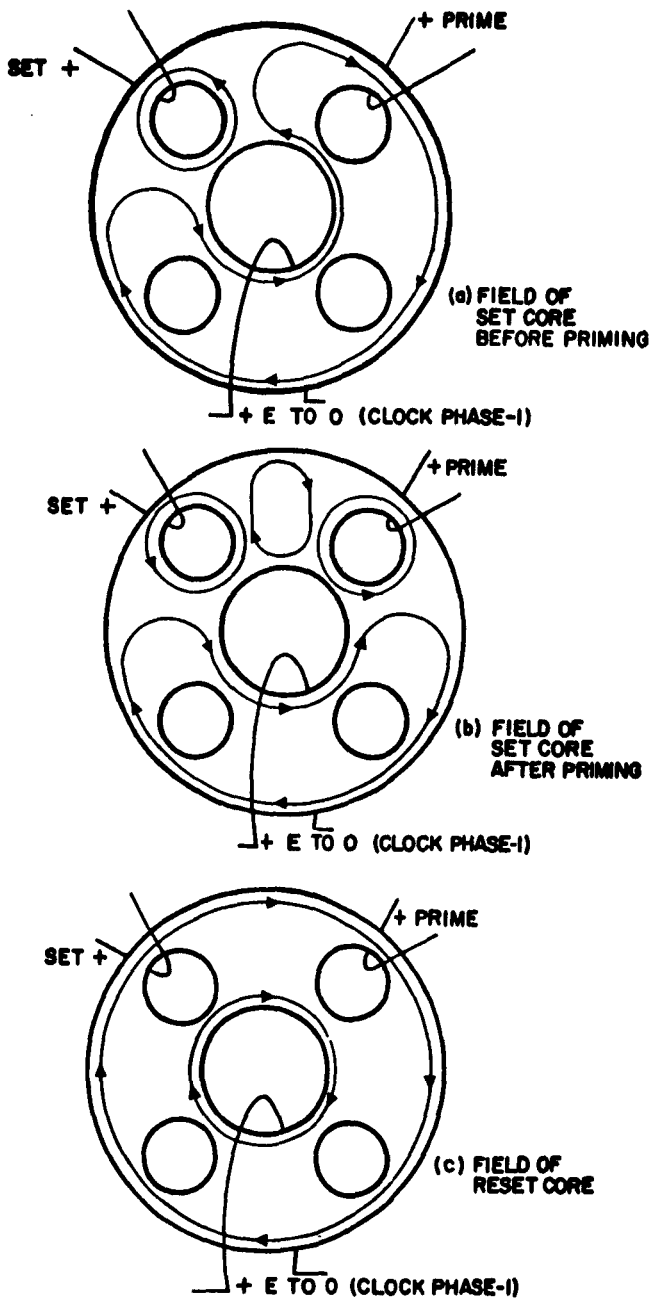


Fig. 2-3 Magnetic Field Conditions of Typical Shift-Register Core

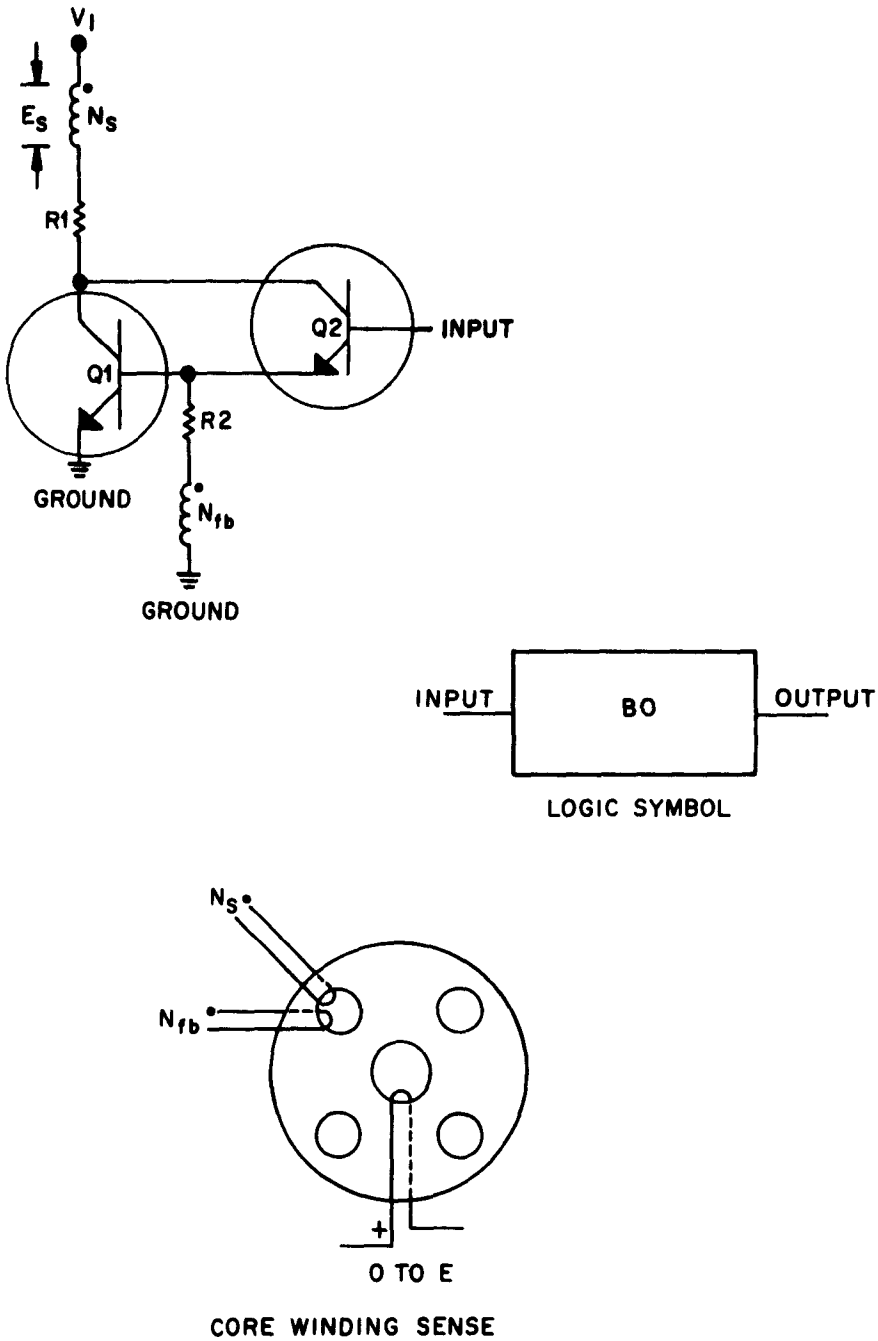


Fig. 2-4 Blocking Oscillator Schematic Diagram

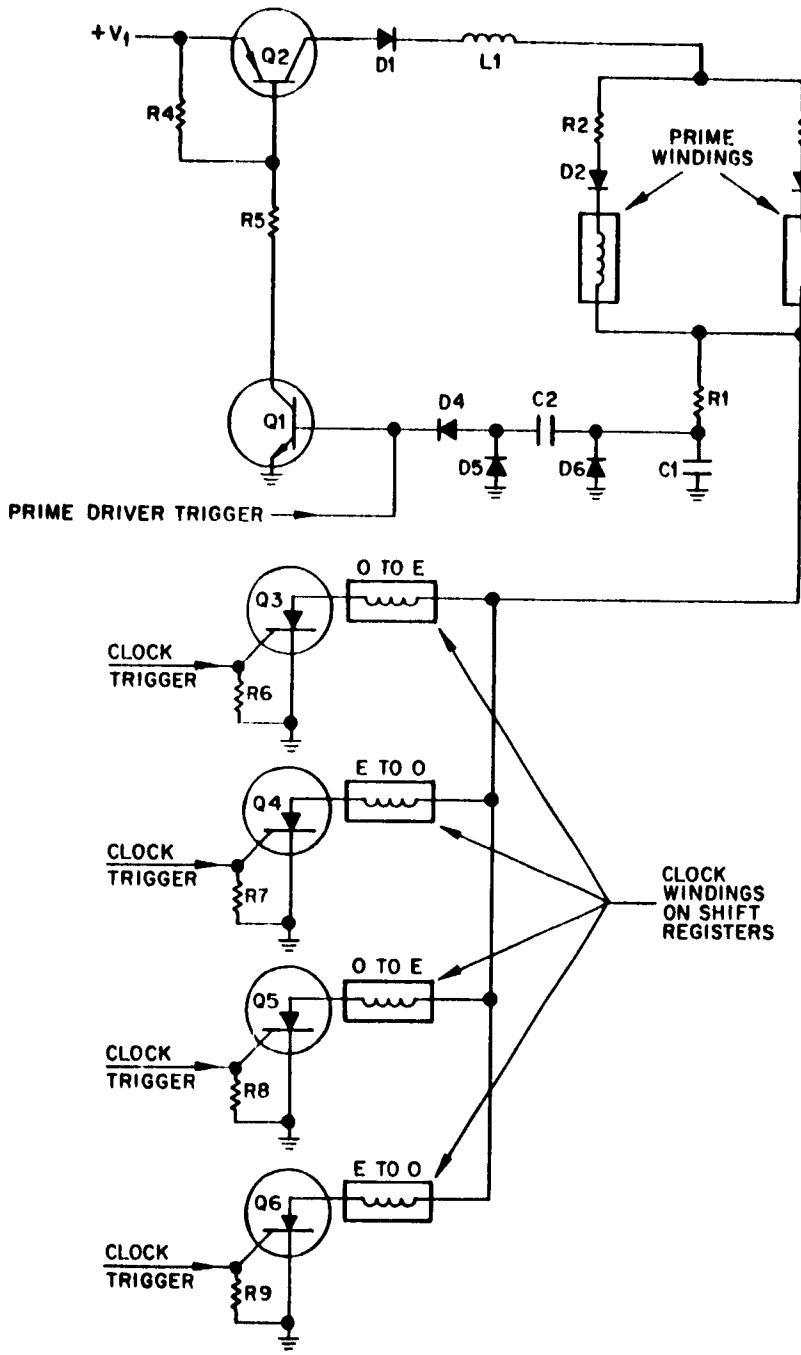


Fig. 2-5 Clock and Prime Driver Schematic Diagram

Operation is initiated when a positive trigger pulse is applied to the base of transistor Q1. This transistor saturates and causes transistor Q2 to saturate. In effect, this places the power supply across the series circuit consisting of L1, C1, R1, R2 and R3 in parallel, and the prime windings in parallel. The current flowing in this resonant network approximates a half sinusoid with a period proportional to $\sqrt{L1 \times C1}$. This current is used to prime the shift-register and to charge capacitor C1 to twice the supply voltage. Capacitor C2 supplies the postive feedback necessary to keep transistors Q1 and Q2 saturated until capacitor C1 is fully charged.

After the priming action has been completed, the clock pulse is applied to the shift-register by triggering one of the silicon-controlled-rectifiers, Q3, Q4, Q5, or Q6 into the conduction state. The clock current passing through the silicon-controlled rectifiers is derived from capacitor C1, and the waveform is shaped by resistor R1. The complete discharge of C1 turns off the silicon-controlled rectifier, and the circuit is ready to be primed again.

2.5 VOLTAGE SWITCH

The voltage switches sample the state of the shift-register and feed an 800 cps signal into the ladder-adder. The voltage switch requirements are twofold:

(1) To present the same impedance to the ladder-adder when in either the "1" or the "0" state

(2) To have memory capability; this is necessary because the shift-register, when sampled, produces a 0.5 μsec pulse, whereas, a continuous signal is required from the voltage switches.

A circuit which satisfies the above specifications is shown in Fig. 2-6. The impedance criterion is satisfied by having the PNPN switch conduct for the "1" condition and having the diode conduct during the "0" condition. The memory requirement is satisfied by the inherent bistable characteristic of the PNPN switch.

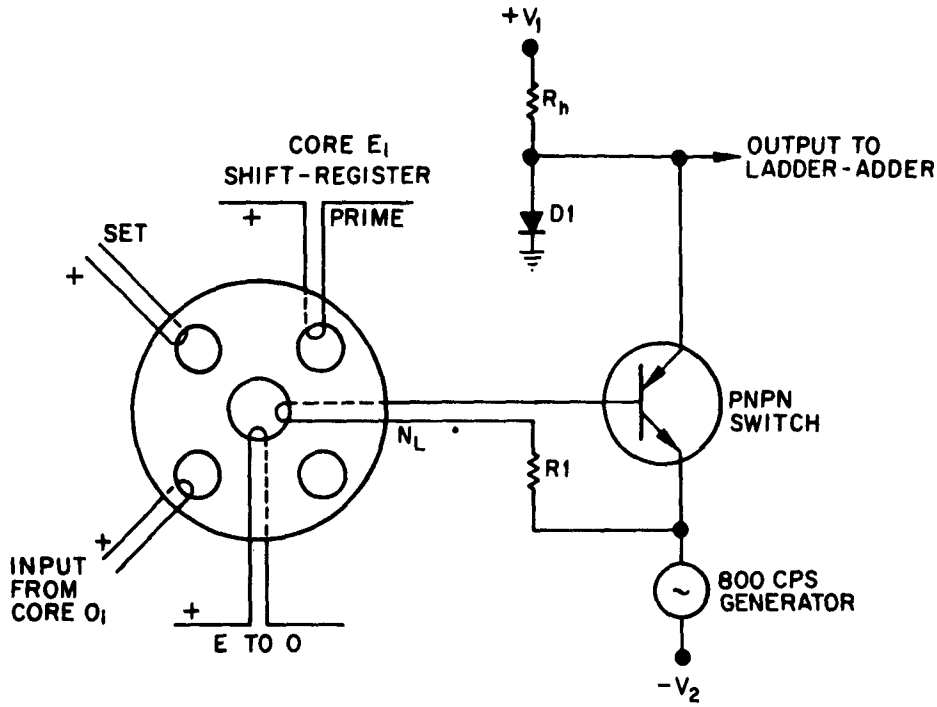


Fig. 2-6 Typical Voltage Switch Schematic Diagram

The circuit is activated by a pulse from the shift-register applied to the base of the PNPN switch. A positive pulse turns the PNPN switch on (denoting a "1" for that particular bit from the shift-register) and a negative pulse turns the PNPN switch off (denoting a "0" for that particular bit of the shift-register). The PNPN switch requires a certain minimum current in order to remain in conduction. This current is delivered by power supplies V_1 and $-V_2$ through resistor R_h. When the PNPN switch is on, the anode is essentially at voltage $-V_2 + V_{800\ cps}$. This voltage is always negative with respect to ground, since V_2 is always greater than $V_{800\ cps}$, and serves to reverse-bias the silicon diode D1. When the PNPN switch is turned off, the diode D1 becomes forward biased to ground and conducts the current from power supply V_1 through resistor R_h. This current is selected so that the ac impedance of the diode is equal to the ac impedance of the PNPN switch.

2.6 LADDER-ADDER

The ladder-adder circuit converts the digital information presented by the voltage switches into the desired analog signal, i.e., an 800 cps voltage. The ladder-adder (Fig. 2-7) presents the same input impedance to each switch position, namely 15K ohms. To understand how the ladder-adder achieves digital-to-analog conversion, assume that an ac voltage (800 cps) is injected by switch 1. Two-thirds of this voltage is developed across resistor R_4, and the remaining one-third appears across the ladder network. This remaining third of the voltage is then successively divided by two at each node of the ladder.

The last resistor in the ladder, R21, is connected to the virtual ac ground at the input to a summing amplifier. Thus, the contribution of switch 1, which the summing amplifier sees, is proportional to 1/3 × 1/512 of the ac voltage injected. By a similar process, switch 2 contributes 1/3 × 1/256 of the initial voltage it injects. The net result is an 800-cps voltage which is directly proportional to the sum stored in the shift-register.

2.7 10-COUNT MAGNETIC SCALER

The 10-count magnetic scaler (Ref. 5) is built with square-loop magnetic cores. This magnetic scaler, Fig. 2-8, counts ten cycles of input voltage from the clock and fires, resetting the flip-flops and preparing the system for the next data input. The term "ladle and bucket" is aptly applied to this counter circuit. A discrete electrical quantity is generated (the filled ladle) and then dumped into a reservoir of definite capacity (the bucket). Overflow from the reservoir is sensed by a circuit which empties the reservoir and gives a count of the number of times the ladle is dumped into the bucket.

The electrical quantity generated is a voltage pulse whose volt-time integral is proportional to the magnetic flux switched in square-loop core T1. This switched flux is

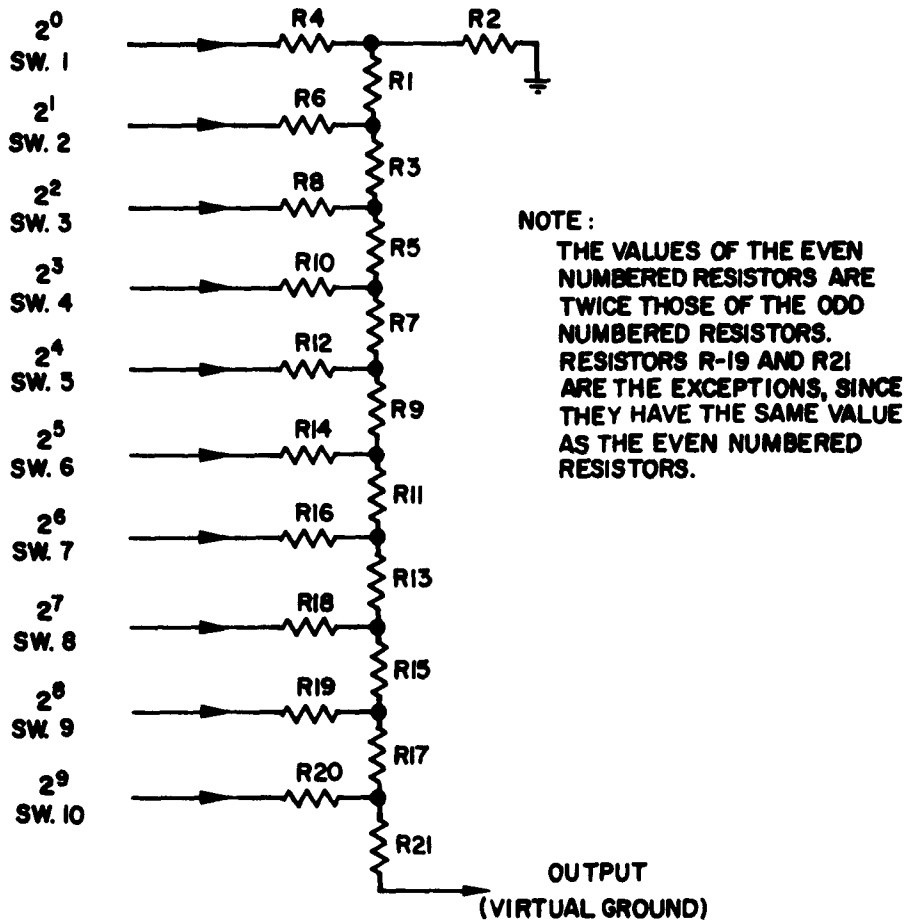


Fig. 2-7 Ladder-Adder Network Schematic Diagram

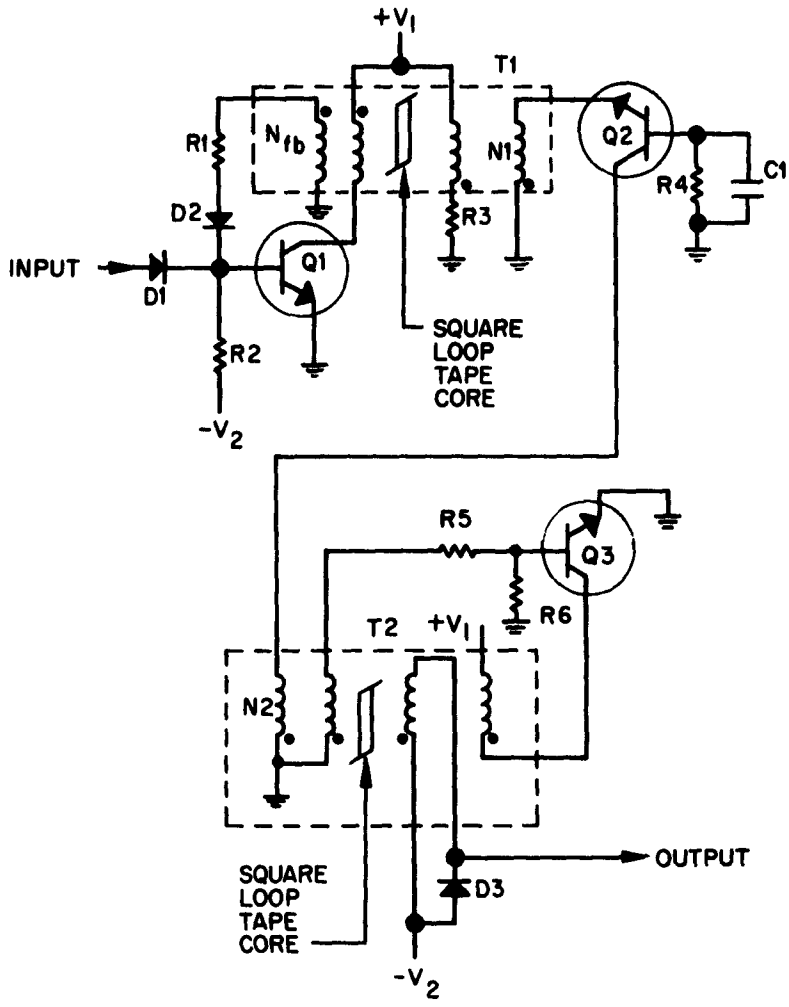


Fig. 2-8 10-Count Magnetic Scaler Schematic Diagram

constant for a given core, from which it follows that the volt-time integral $\int vdt$ is also constant. Thus, the electrical quantity is the output voltage produced by switching square-loop core T1. The switching action is initiated by a positive trigger applied to the base of transistor Q1 which causes the transistor to saturate. The transistor remains saturated because the feedback voltage generated in winding N_{fb} holds the base positive until the core T1 is completely switched. At this time, the windings are no longer capable of supporting a voltage and the transistor is turned off. The core is then reset with direct current which is limited by resistor R3.

The reservoir utilized is the switchable flux of square-loop core T2. The output from core T1 is coupled through transistor Q2 to core T2. The turns ratio of these two core windings, N_1 and N_2, are chosen so that one-tenth of the flux in core T_2 is switched every time core T1 is completely switched. After the tenth input, core T_2 saturates. The state of saturation is detected by transistor Q3 which resets core T2 and also provides the output signal.

2.8 INTERNAL CLOCK

The internal clock consists of two square-wave trains, 180° out of phase with each other. These signals are generated by a type of circuit commonly referred to as a dc-to-ac converter (Ref. 6). The frequency of oscillation is determined by the flux capacity of square-loop core T1 and the power supply voltage $+V_1$ (Fig. 2-9). This particular circuit is designed to operate at 2kc with a square-wave output swing of ±4 volts about ground.

The two transistors Q1 and Q2 operate in push-pull, with the core windings arranged to provide positive feedback from the collector of each transistor to its base. Capacitor C1 suppresses transient voltage spikes which could damage the transistors. Resistors R1 and R2 are selected to forward bias the transistors (making the circuit self-starting) and to satisfy the base drive requirements. Thus, when the power is turned on, the higher gain transistor (assumed to be Q1) saturates. In saturating, it turns off transitor Q2 because of the negative voltage induced in the base feedback

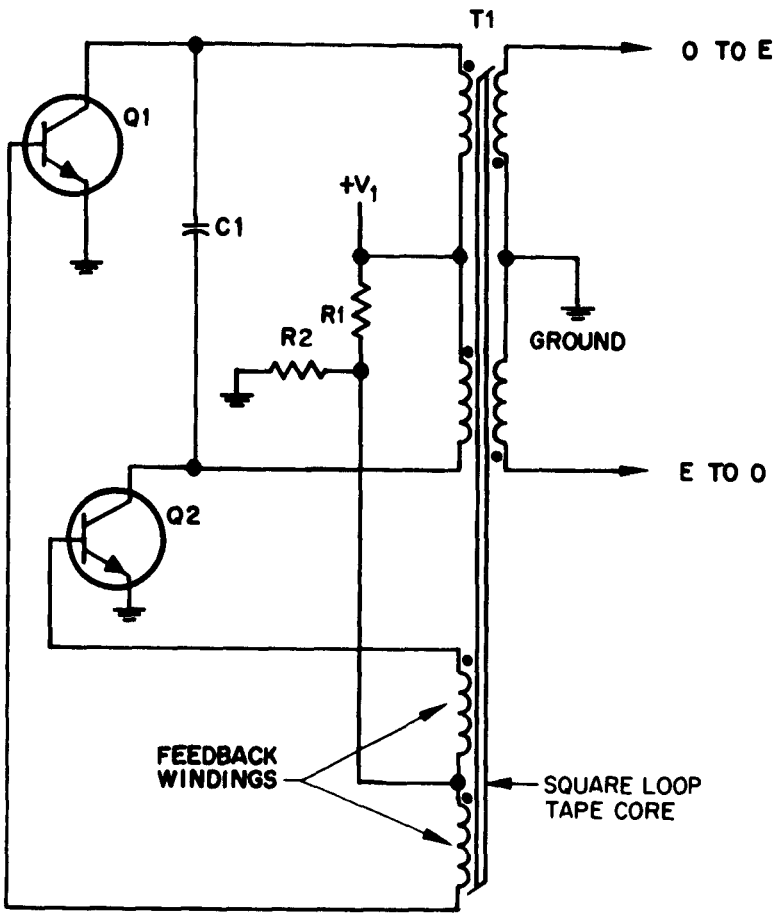


Fig. 2-9 Internal Clock Schematic Diagram

winding of transistor Q2. This condition continues until core T1 saturates. Now the primary inductance of T1 is reduced by at least four orders of magnitude because of the change in permeability. The windings are no longer capable of sustaining a voltage, and transistor Q1 begins to turn off due to lack of base drive. The magnetic field stored in the leakage inductance of each winding collapses at this point. This generates a voltage in the feedback windings such that transistor Q1 turns off faster and transistor Q2 begins to turn on. Once the core begins to switch again, positive feedback turns off transistor Q1 and maintains transistor Q2 at saturation. The core is now switched back to its original saturation state. When the core becomes saturated again, the transistors once more change state.

2.9 OR GATE

The output of an OR gate (Ref. 7) is logically TRUE if any one input is TRUE. When all inputs are FALSE (-3 volts or less), the output is FALSE. For this particular system, a TRUE signal is +3 volts or greater, and a FALSE signal -3 volts or less. A multi-input OR gate is shown in Fig. 2-10. When all of the circuit inputs are FALSE, the circuit output terminal (which is the common node for the cathodes of diodes D_A, $D_B, \ldots, D_N$) is FALSE. When one or more of the inputs is TRUE, the output is TRUE.

2.10 AND GATE

The output of an AND gate (Ref. 7) is TRUE only when all inputs are TRUE. One or more FALSE inputs produce a FALSE output. A multi-input AND gate is shown in Fig. 2-11.

One or more FALSE input signals cause diodes on the inputs to be forward-biased, holding the AND gate output at the FALSE voltage level. When all inputs are TRUE, all diodes become reverse-biased, thereby allowing the gate output to rise to the TRUE level.

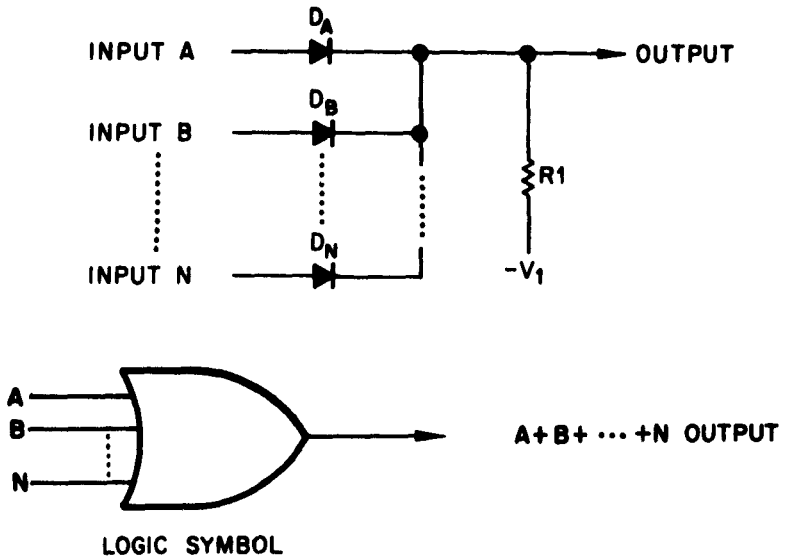


Fig. 2-10 Typical OR Gate Schematic Diagram

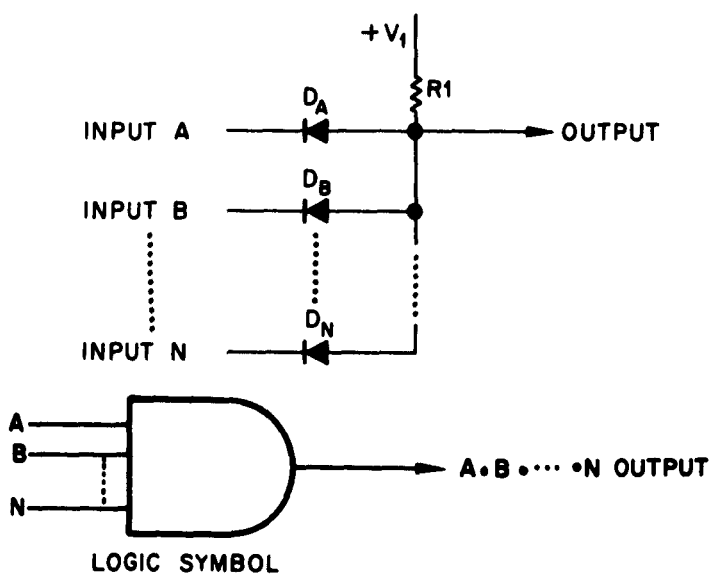


Fig. 2-11 Typical AND Gate Schematic Diagram

2.11 DIFFERENTIATING GATE

The circuit used to perform the differentiation function appears in Fig. 2-12. Because of the relatively high impedance level of the diode gates, an inductor was considered to be a more suitable element than a capacitor to perform this function.

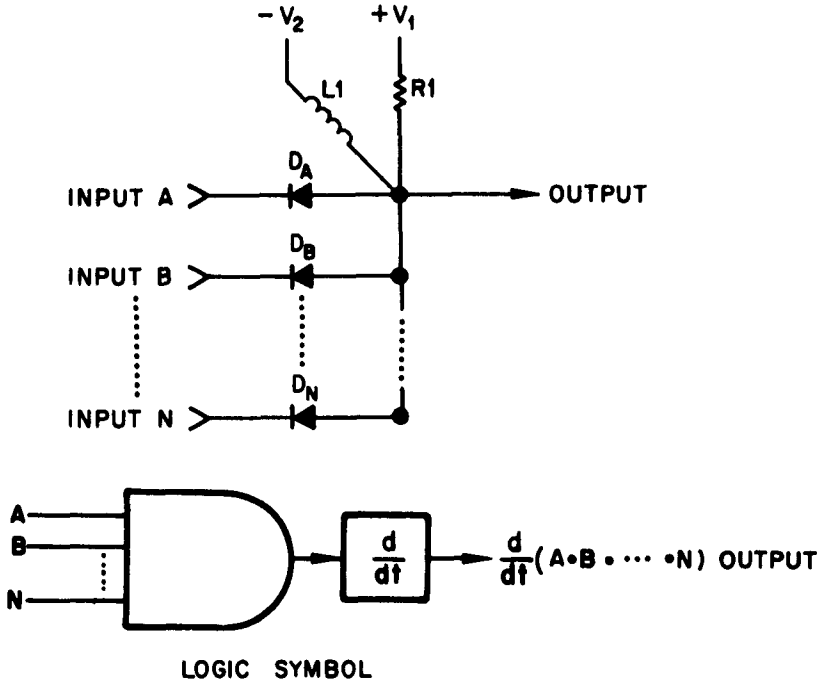


Fig. 2-12 Typical Differentiating Gate Schematic Diagram

The circuit operation is as follows. A FALSE input to the gate acts like a sink, drawing all of the current flowing through resistor R1. When all the inputs are TRUE, the inductor develops a back voltage which instantaneously prevents inductor current from flowing. Thus, the output becomes TRUE and the current through resistor R1 is now supplied to the load. After the first instant of time, the voltage across the inductor decays in accordance with the L/R time constant (where R is an equivalent resistance

consisting of R1 and the load). This decay becomes complete when all of the current from R1 flows through the inductor. In the above fashion, all TRUE inputs result in a differentiated TRUE output.

2.12 FLIP-FLOP

The flip-flop is a bistable logic circuit (Ref. 7). The type used in this system (Fig. 2-13) consists of two transistors which are cross-coupled in order to supply the required positive feedback. This circuit is commonly referred to in the literature as an R-S (reset-set) flip-flop or as two cross-coupled gates.

The "0" output is TRUE when the flip-flop is reset. The "1" output is FALSE for this condition. When the flip-flop is set, the "1" output is TRUE and the "0" output is FALSE.

The circuit operation is as follows. Assume that the flip-flop is reset, i.e., the "1" output is FALSE. Transistor Q2 is saturated and transistor Q1 is turned off. A positive (TRUE) pulse is now applied to one of the set inputs of the flip-flop and transistor Q1 saturates. Resistors R3 and R4 now act as a voltage divider network which reverse-biases transistor Q2 and turns it off. Thus, the "1" output of the flip-flop is now TRUE and the "0" side FALSE. To reset the flip-flop, a positive (TRUE) pulse is applied to one of the reset inputs.

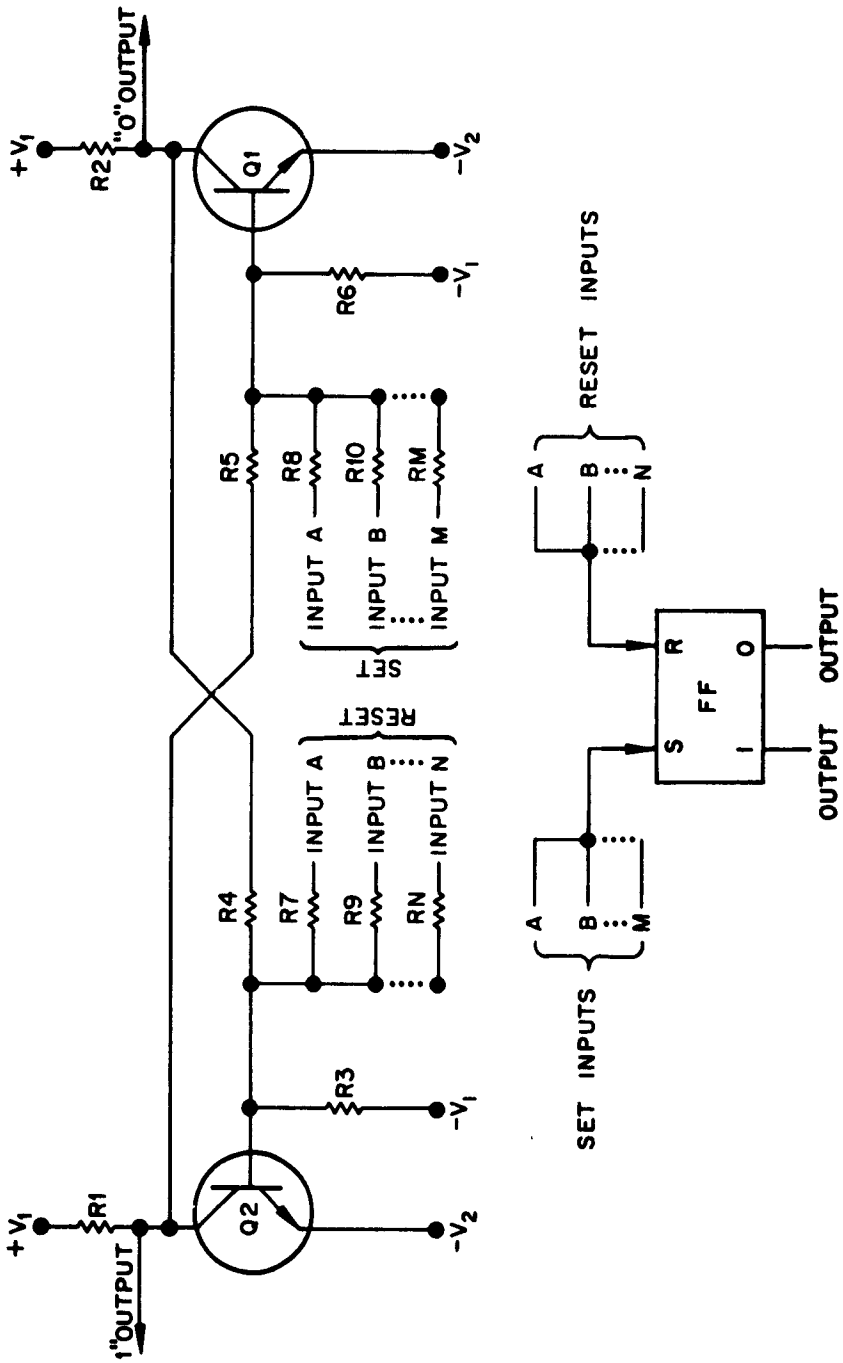


Fig. 2-13 Typical Flip-Flop Schematic Diagram

Section 3
ERROR ANALYSIS

The system errors are all attributable to the digital-to-analog conversion operation since the digital portions are inherently free of possible error. Therefore, an error analysis need only be concerned with the voltage switches, the ladder-adder network, and the regulation of the 800 cps generator.

The error introduced by the voltage switches is due to their variation in ac impedance. This variation is caused by:

(1) Temperature effects
(2) Differences from device to device
(3) Differences in operating point between the diode and the PNPN switch

The design engineer only has control of items (1) and (3). Item (2) is an inherent characteristic of the device. The error due to item (1) may be reduced by using resistors with appropriate temperature coefficients in the ladder-adder network. Item (3) is discussed below.

For the purpose of this discussion, the equivalent circuit is used (Fig. 3-1). The active elements of Fig. 2-6 have been replaced by their equivalent impedances (Z_d and Z_{PNPN}) and a SPDT switch. Resistor R_h and power supplies V_1 and $-V_2$ are used to select the operating points of the active elements, and R_{in} is the input impedance of the ladder.

The impedance, seen looking back into the ladder from a particular switch, is:

$$Z = \frac{R_{in} R_h}{R_{in} + R_h} \qquad (1)$$

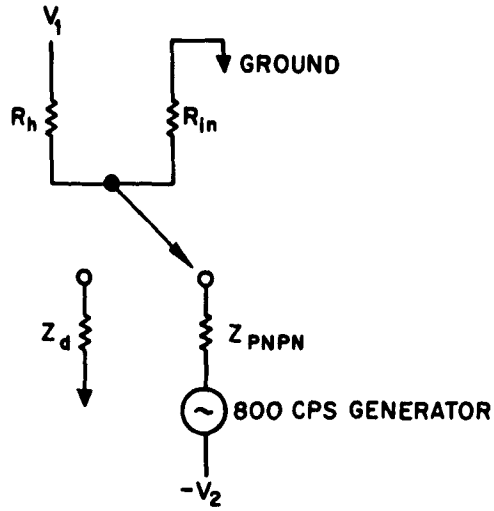


Fig. 3-1 Voltage Switch Equivalent Circuit Diagram

The fractional error introduced by the switches is then given by:

$$\text{Error} = \Delta Z_{sw} \Big/ \frac{R_{in} R_h}{R_{in} + R_h} \tag{2}$$

where ΔZ_{sw} is the variation in the ac impedance of the switches from their nominal value, due to items (1), (2), and (3) above. For an accuracy requirement of ± 0.1 percent, the above expression becomes an inequality:

$$\Delta Z_{sw} \leq 1 \times 10^{-3} \frac{R_{in} R_h}{R_{in} + R_h} \tag{3}$$

The values of R_{in} and R_h are dictated by the system requirements. For this system, R_{in} is 15K ohms due to the specification that the ladder-adder output resistance should be 10K ohms. The value of R_h was selected so that the diode and the PNPN switch operate at points where their respective nominal ac impedances are equal. For the

power supplies and devices used, the value selected is 2.5K ohms. Substituting these values into Eq. (3) yields the allowable variation in ΔZ_{sw}:

$$\Delta Z_{sw} \leq 1 \times 10^{-3} \times \frac{15 \times 10^3 \times 2.5 \times 10^3}{15 \times 10^3 + 2.5 \times 10^3} = 2.14 \text{ ohms} \quad (4)$$

The ac impedance of a sample lot consisting of four 1N646 diodes was measured over the temperature range 0° C to +55° C. This impedance varied between 5.5 and 6.5 ohms. For a sample lot of PNPN switches, the impedance varied between 3.1 and 8.1 ohms. Thus, the largest value of ΔZ_{sw} is 5 ohms. When this value is used in Eq. (2), we obtain:

$$\text{Error } \% = 5 \Big/ \frac{15 \times 10^3 \times 2.5 \times 10^3}{15 \times 10^3 + 2.5 \times 10^3} = \pm 0.23\% \quad (5)$$

which is the accuracy of the voltage switches.

The error introduced by the ladder-adder network is negligible compared to that of the switch. There are ladder-adder networks commercially available which are accurate to to one part in ten thousand.

The 800-cps generator has a dynamic output impedance of 0.14 ohms. This introduces an error given by:

$$\text{Error (800-cps generator) } \% = \frac{I_L \times Z_d}{E_g} \times 100\% \quad (6)$$

where:

I_L is one-half the maximum variation in alternating current
Z_d is the dynamic output impedance of the 800-cps generator
E_g is the nominal 800-cps generator output voltage

For I_L = 15.15 ma, Z_d = 0.14 ohms, and E_g = 3.6 vac, an error of ±0.06 percent is obtained.

The system accuracy is the sum of the errors introduced by the voltage switch, ac generator, and ladder-adder network. Thus, the overall system accuracy is ±0.3 percent. Actual measurements at room temperature yielded an error of less than ±0.25 percent.

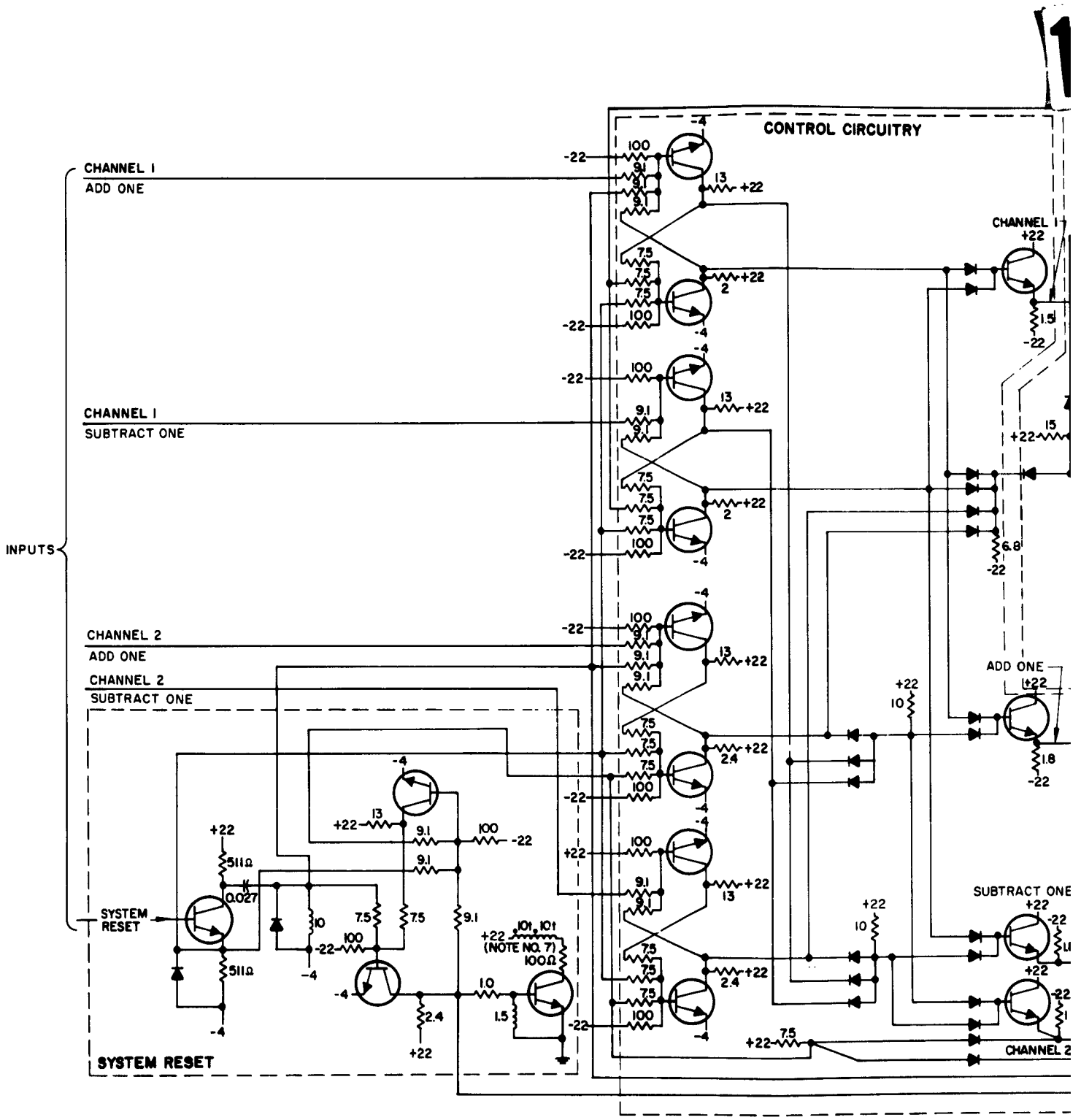
Section 4
SYSTEM OPERATION

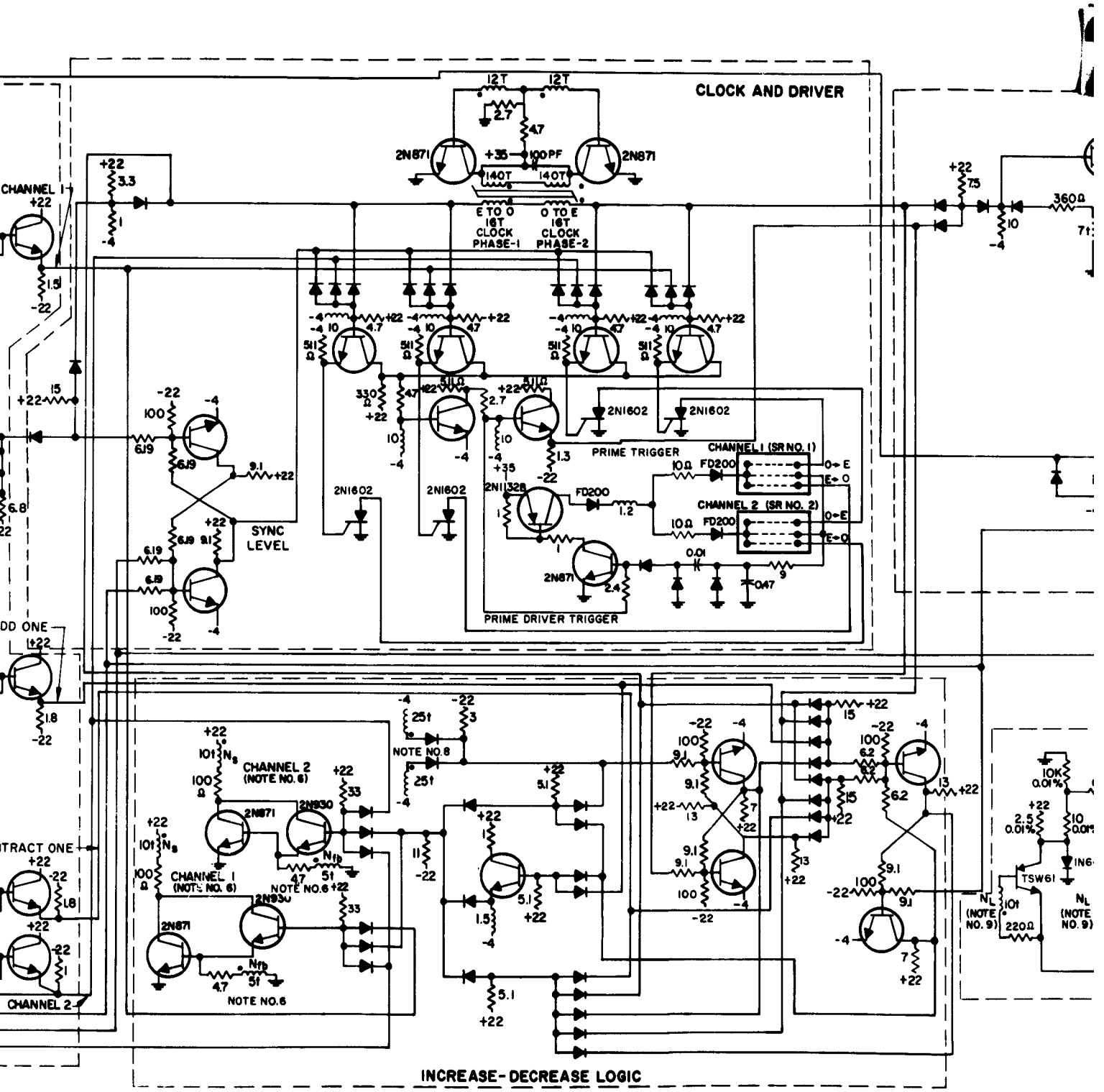
4.1 GENERAL DESCRIPTION

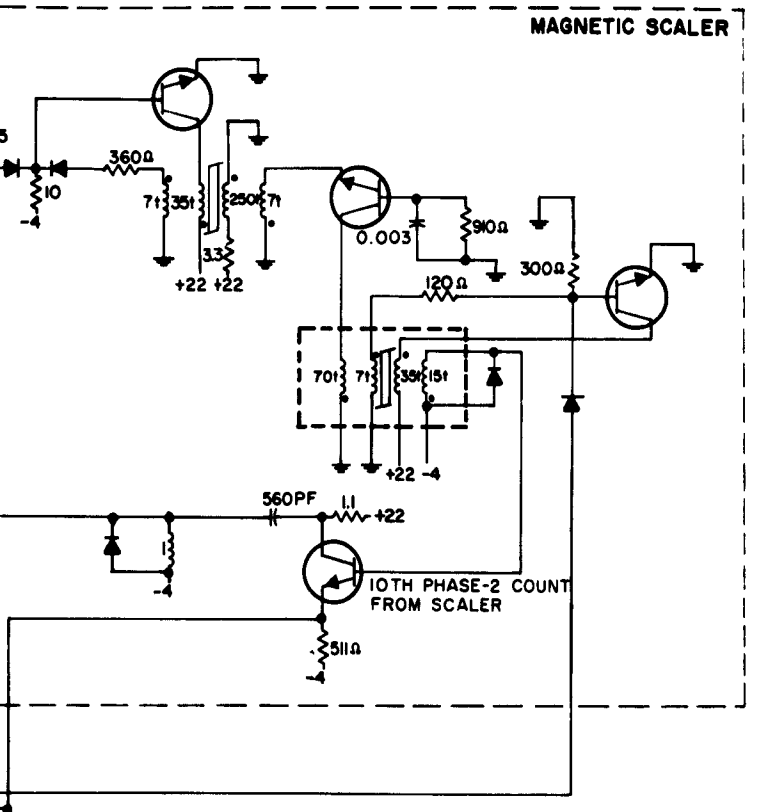
The system schematic appears in Fig. 4-1 and the functional block diagram is given in Fig. 4-2. The equipment has two channels of operation which are continually modified as the result of the input command signals. These signals select the channel to be modified, and they also designate the operation to be performed, i.e., "add one," or "subtract one." This selection process is controlled by flip-flops FF1 through FF4 and OR gates G4 through G7 (Fig. 4-3). Synchronization between the input commands and the internal clock is accomplished by gates G10, G13, and G14 in conjunction with FF5 (Fig. 4-3). The information stored in each channel is then updated by reading out of the shift-register serially, modifying each bit as required, and then reading back into the shift-register serially (Fig. 4-4). The state of the ten-bit shift-registers are sampled at the end of the shifting operation by voltage switches (Fig. 2-6). These switches, in conjunction with a ladder-adder network (Fig. 2-7), convert the digital sum into an analog voltage which is directly proportional to this sum.

Figure 4-2 illustrates the system operation and shows the basic elements used in the system mechanization. These elements are:

- Time-sharing control logic
- Internal clock
- 10-count magnetic scaler
- Increase-decrease logic
- Shift-register drivers
- All-magnetic shift-registers
- Voltage switches

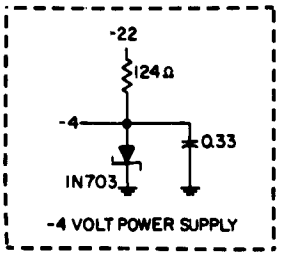

CONTROL CIRCUITRY
INPUTS
CHANNEL 1
ADD ONE
CHANNEL 1
SUBTRACT ONE
CHANNEL 2
ADD ONE
CHANNEL 2
SUBTRACT ONE
SYSTEM RESET
SYSTEM RESET
(NOTE NO. 7)
CHANNEL 1
ADD ONE
SUBTRACT ONE
CHANNEL 2

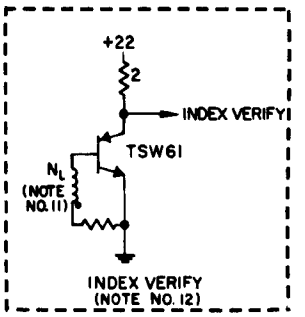

CLOCK AND DRIVER
CHANNEL 1
2N871
E TO O 16T CLOCK PHASE-1
O TO E 16T CLOCK PHASE-2
2N1602
PRIME TRIGGER
PRIME DRIVER TRIGGER
CHANNEL 1 (SR NO. 1)
CHANNEL 2 (SR NO. 2)
FD200
SYNC LEVEL
CHANNEL 2 (NOTE NO. 6)
CHANNEL 1 (NOTE NO. 6)
2N930
NOTE NO. 6
NOTE NO. 8
INCREASE-DECREASE LOGIC
CHANNEL 2
TSW61



NOTES:

1. ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ALL RESISTANCE VALUES IN KILOHMS UNLESS OTHERWISE SPECIFIED
3. ALL INDUCTANCE VALUES IN MILLIHENRIES UNLESS OTHERWISE SPECIFIED
4. ALL TRANSISTORS 2N2087 UNLESS OTHERWISE SPECIFIED
5. ALL DIODES PD307 UNLESS OTHERWISE SPECIFIED
6. THESE WINDINGS ARE ON THE FIRST E CORE OF EACH SHIFT – REGISTER SEE FIG. 2-4 FOR WINDING SENSE
7. THESE WINDINGS ARE USED TO INDEX THE SHIFT – REGISTERS TO A PREDETERMINED COUNT. THEY ARE PLACED ON THE O CORES TO BE SET THE WINDING SENSE IS SHOWN IN FIG. 2-4
8. THESE WINDINGS ARE ON THE TENTH E CORE. THE WINDING SENSE IS SHOWN IN FIG. 2-1
9. THESE WINDINGS ARE ON EVERY E CORE OF BOTH SHIFT REGISTERS. THE MOST SIGNIFICANT BIT IS STORED IN CORE E_1 AND CORRESPONDS TO THE SWITCH LABELED 2^9. SEE FIG. 2-1 AND FIG. 2-6 FOR THE WINDING SENSE
10. THERE ARE TWO SETS OF TEN SWITCHES, ONE SET PER SHIFT – REGISTER
11. THIS WINDING IS ON THE INDEXED CORE. SEE FIG. 2-6 FOR THE WINDING SENSE
12. THERE ARE TWO INDEX-VERIFY CIRCUITS, ONE FOR EACH SHIFT – REGISTER





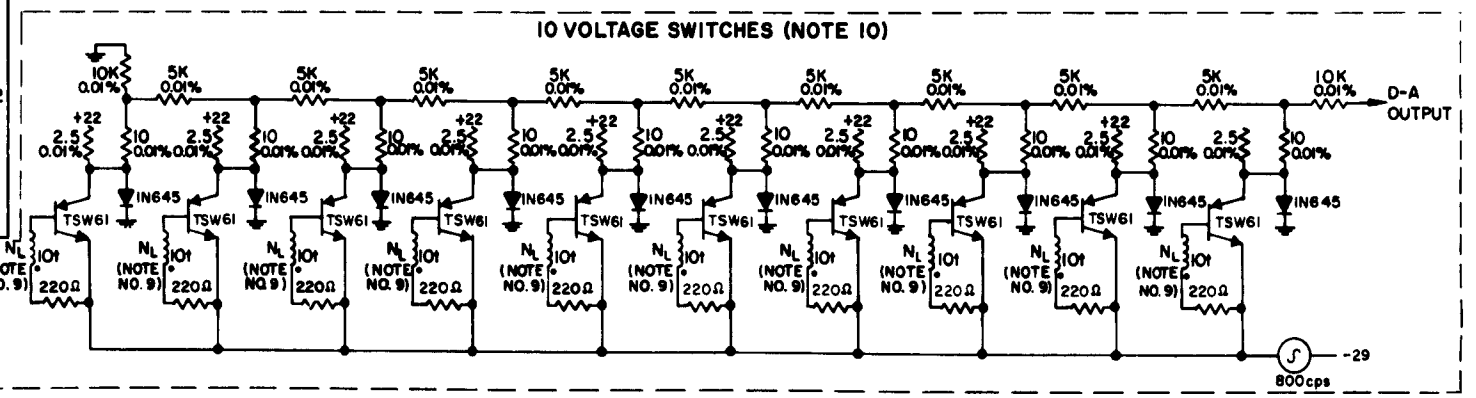


Fig. 4-1 System Schematic Diagram

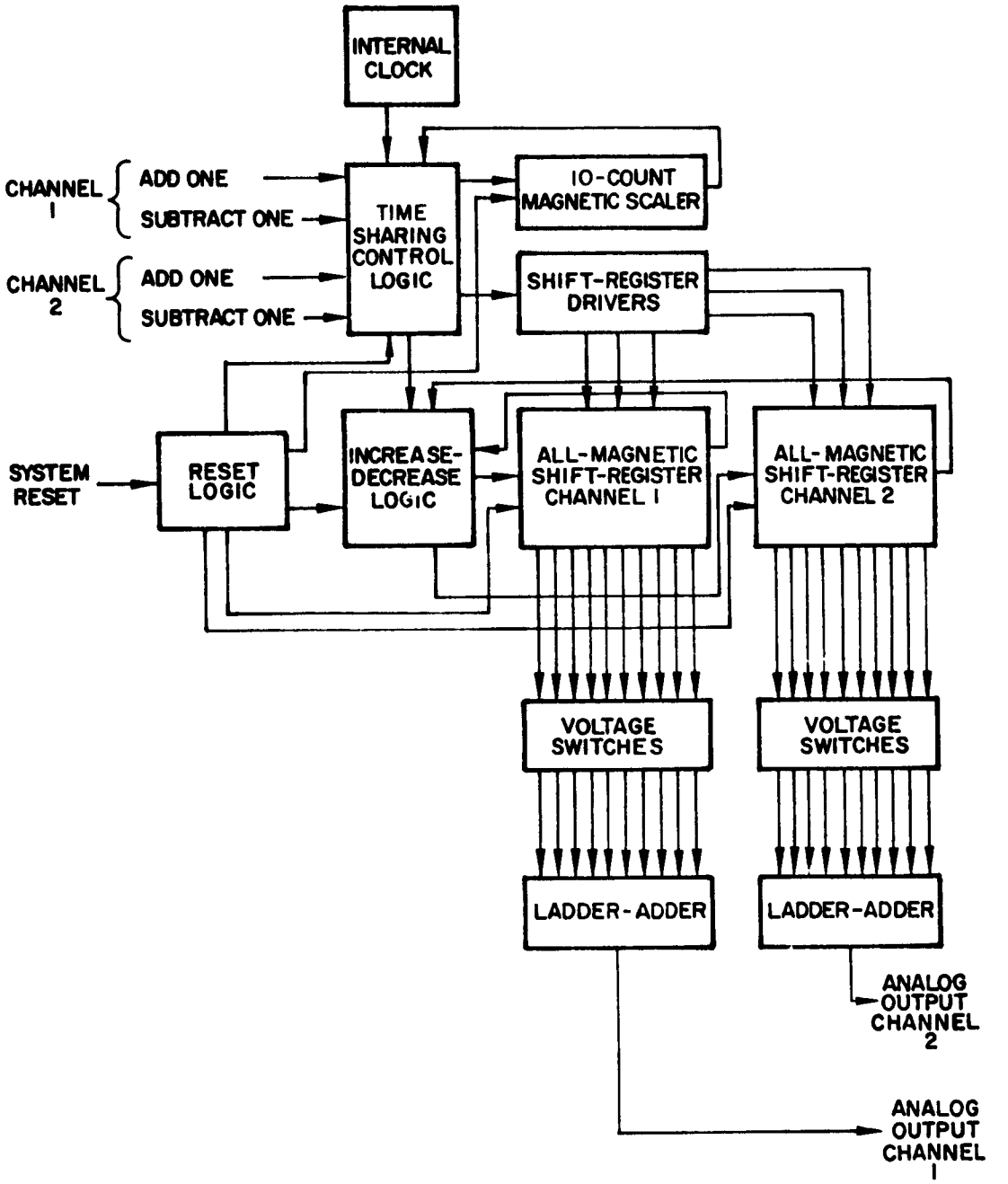


Fig. 4-2 System Functional Block Diagram

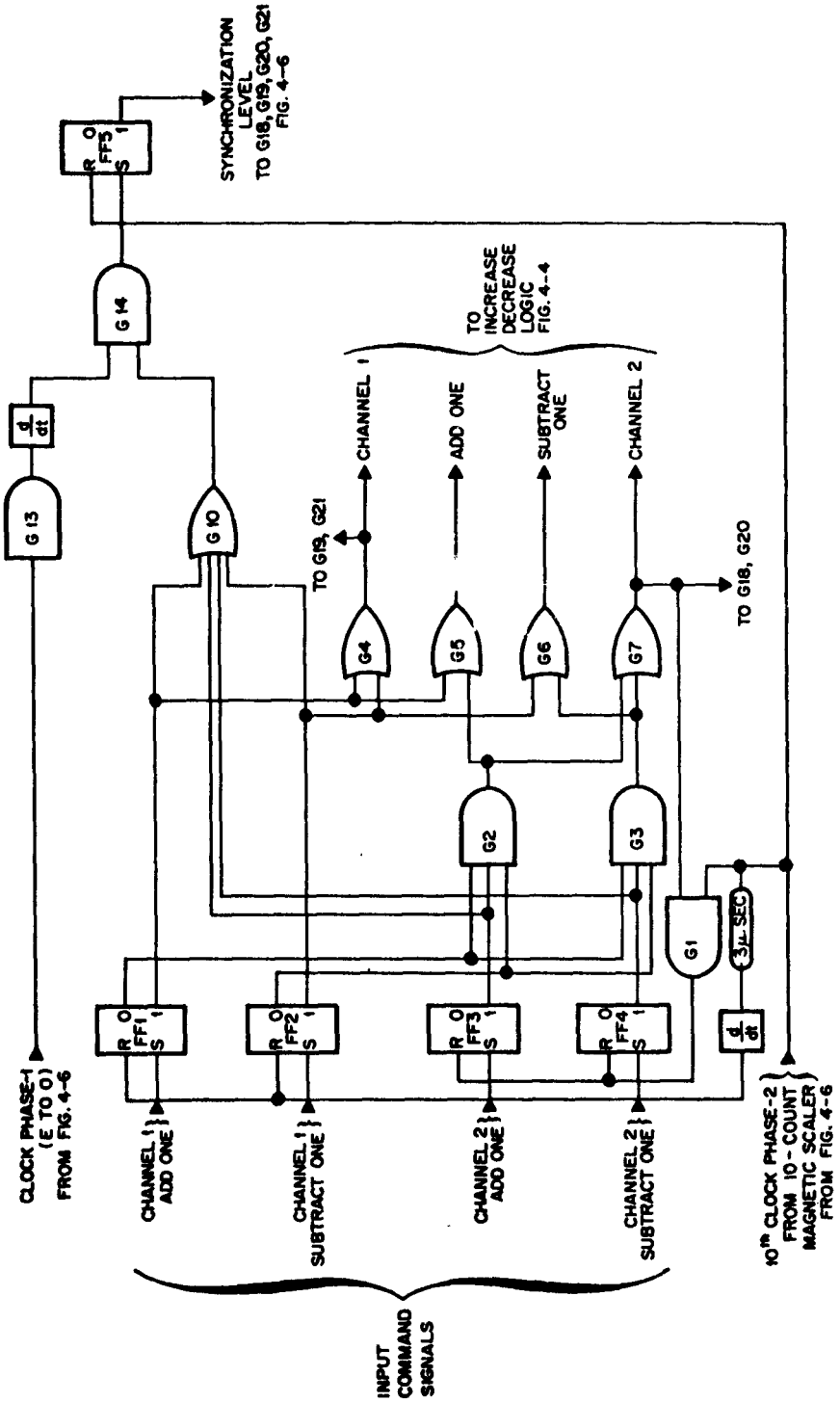


Fig. 4-3 Time-Sharing Control Logic Diagram

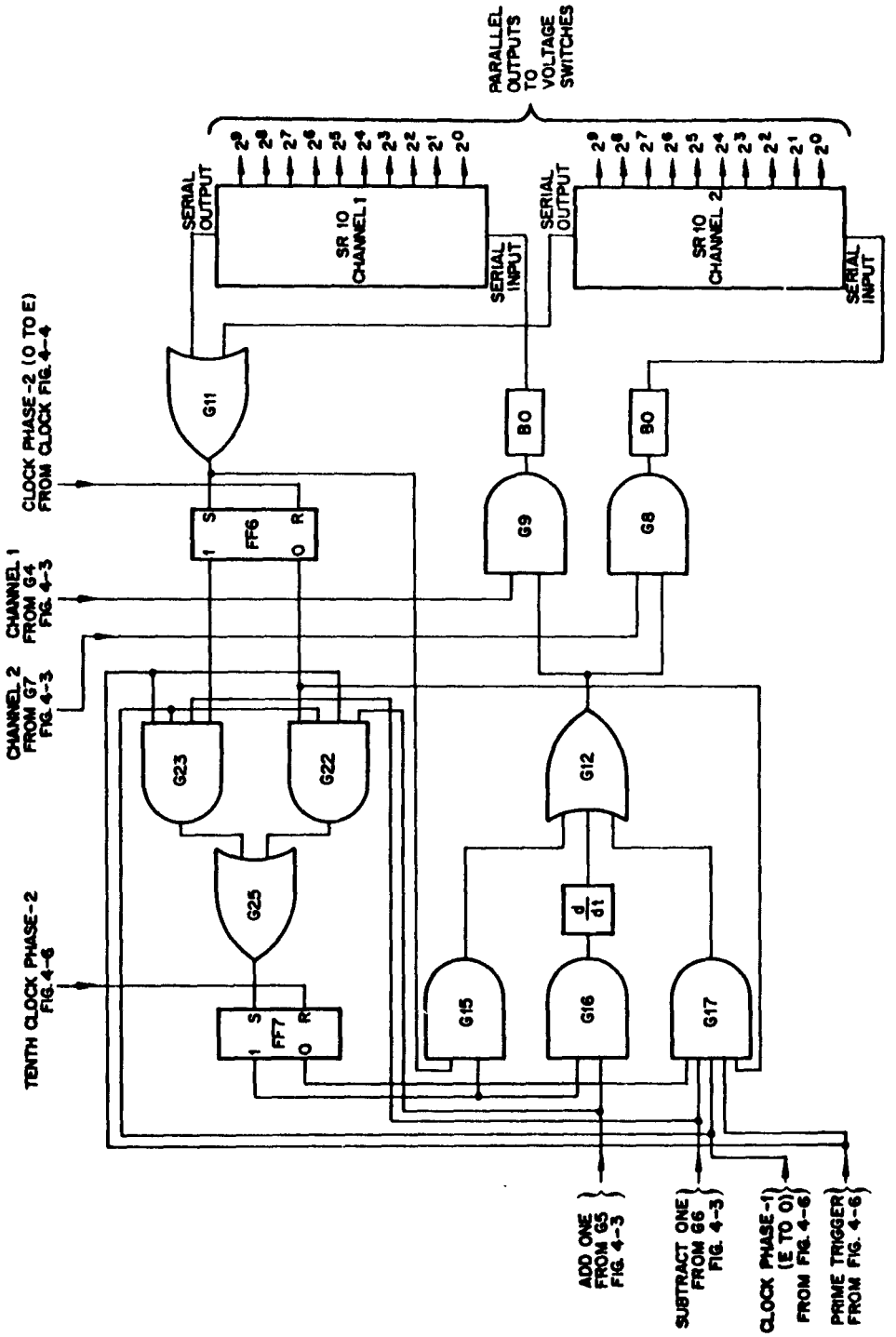


Fig. 4-4 Increase-Decrease Logic Diagram

- Ladder-adder
- Reset logic

The operation proceeds in the following manner. A command pulse is received, requiring the count stored in one of the two magnetic shift-registers to be increased or decreased by unity. The control logic synchronizes and gates the internal clock; sets up the appropriate operation, i.e., addition or subtraction; selects the proper channel to be modified; and begins stepping the 10-count magnetic scaler. The contents of the shift-register are then shifted into the increase-decrease logic. The increase-decrease logic operates on each bit, as required, and transfers the modified bit into the shift-register before the next clock time. This summing operation is completed after the 10th clock cycle, at which time the 10-count magnetic scaler resets the logic to a standby condition. A winding around the major aperture of the E cores (Fig. 2-1) of the shift-register is connected to the trigger input of a PNPN switch. The states of these switches after the tenth clock time are the same as the cores by which they are controlled. Thus, a closed switch denotes a logical "1" in the shift-register for that particular bit. The switches inject an 800-cps voltage into a ladder-adder network. This network sums the voltage contribution from each bit and yields an 800-cps voltage directly proportional to the digital sum present in the shift-register.

4.2 INPUT SIGNALS

Figure 4-5 represents the time relationships between input commands. This timing diagram shows that the input signals may occur only at the beginning of a 10-ms time interval and that for any given interval there might be no signals present. When input commands to both channels occur during the same time interval, the input signal for channel 1 precedes the signal for channel 2 by at least 1 μsec. This condition is necessary to ensure that the operation performed by channel 1 has been completed before any operations are performed on channel 2.

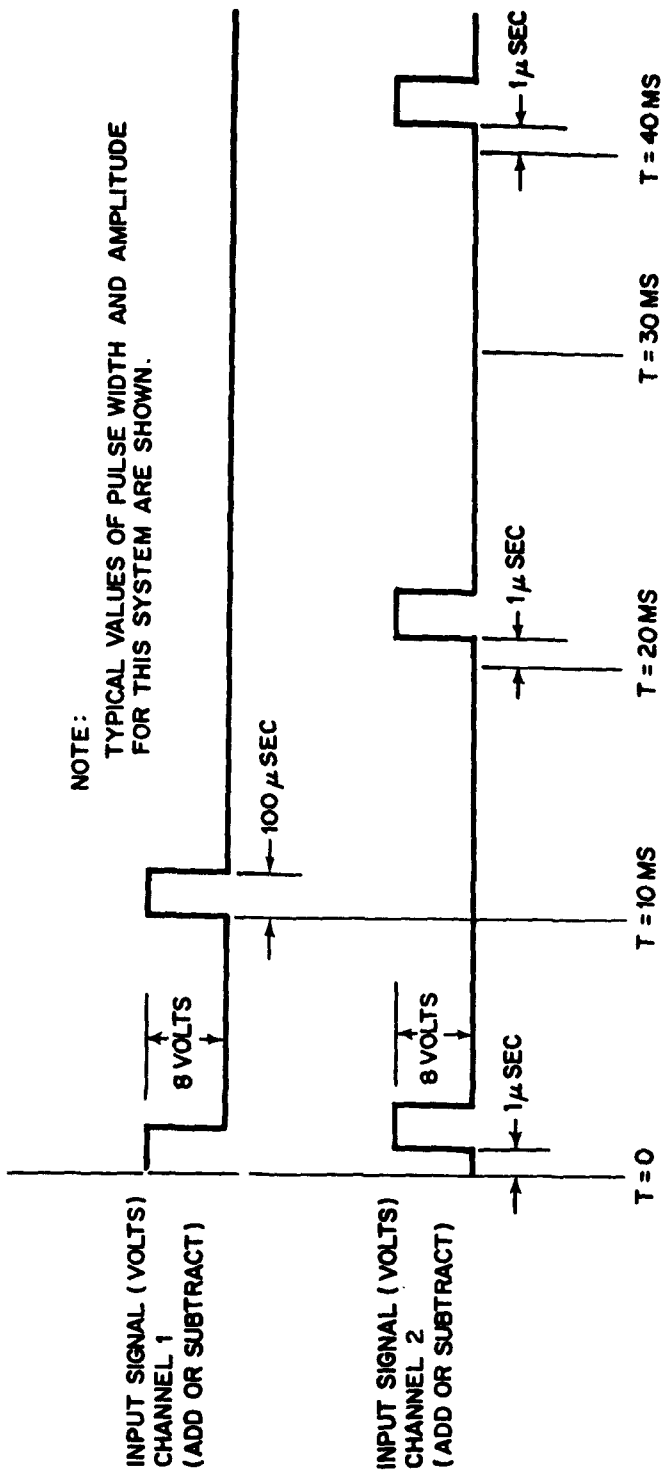


Fig. 4-5 Timing Relationships of Input Command Signals

The maximum repetition rate of the command signals is 100 cps; i.e., the count in each channel may be increased or decreased every 10 ms. This limitation is imposed by the shift-register driver circuit. The ultimate frequency limitation for a 10-bit word length is 1,000 cps, imposed by the magnetic shift-registers.

4.3 TIME-SHARING CONTROL LOGIC

A detailed block diagram of the control logic circuitry is shown in Fig. 4-3. Assume that the input command to channel 1 is "add one." Flip-flop 1 is set, which in turn forces the signals channel 1 (G4) and "add one" (G5) to be TRUE, while maintaining the signal channel 2 (G7) and "subtract one" (G6) FALSE. Synchronization of the internal clock with the input command is obtained by ANDing the leading edge of clock phase-1 (E to O) with the output of G10 at G14. The output of G10 is TRUE because FF1 has been set by the input command "add one" in channel 1. This operation ensures that FF5 will always be set at the beginning of clock phase-1 (E TO O), thereby preventing a half-pulse condition from arising.

Assume that the input command for channel 1 is "add one" and for channel 2 "subtract one," and that these occur in the same cycle. Flip-flop 4 is set 1 μsec after FF1. The operation proceeds as in the previous example. Flip-flop 1 is reset after the tenth clock phase-2 (O to E), but FF4 is not reset since G7 is FALSE. This gate will remain FALSE until FF1 is reset. However, by the time FF1 is reset, the reset signal will be FALSE, thus preventing FF4 from being reset. Synchronization is now accomplished in the same manner as described above except that G10 is now TRUE because FF4 instead of FF1 has been set by the new input command. Flip-flop 4 is then reset after the tenth clock phase-2 (O to E).

4.4 INTERNAL CLOCKING

The internal clock is a free-running oscillator which uses a square-loop tape core to determine the frequency. The control logic permits either G18 and G20,or G19 and G21

(Fig. 4-6) to be clocked TRUE. The gated clock is then differentiated to obtain a 10 μsec pulse. This signal is used to turn on a silicon-controlled-rectifier which drives one of the magnetic shift-registers. The differentiated clock signal is then delayed 60 μsec, inverted, and differentiated again to develop the prime-driver trigger for the shift-registers. This signal is then differentiated and applied with clock phase-2 signal (O to E) in G27 which steps the 10-count magnetic scaler. The scaler output which occurs after the tenth phase-2 prime trigger is used to reset the system indicating the end of a computation.

4.5 INCREASE-DECREASE LOGIC

The increase-decrease logic is time-shared and makes use of the following algorithms (Ref. 8) in order to add unity to or subtract unity from the number in the shift-registers. To add unity, "0's" are shifted into the register until the first "0" out of the register is sensed; then this bit is changed to a "1" and shifted back into the register. All succeeding bits are shifted back into the register unmodified. To subtract unity, the procedure is reversed, i.e., "1's" are shifted into the register until the first "1" out of the register is sensed; then this bit is changed to a "0" and shifted back into the register. All succeeding bits are shifted unmodified back into the register.

Figure 4-4 shows the implementation of the increase-decrease logic. Asume it is required to "add one" to binary number, 0000010111, which is stored in shift-register channel 1. The least significant bit is shifted out of the register by clock phase-1 and sets FF6. Gates G15 and G16 are inhibited by FF7 which is in the reset state. Gates G17 and G23 are each inhibited by the signal "subtract one," which is FALSE during the addition operation. Gate 22 is TRUE when its four inputs are TRUE.

Since the first bit set FF6, G22 is FALSE and FF7 remains reset during the first clock cycle. Thus, a logical "0" has been put into the most significant bit position of the shift-register. The second and third bits of the example are logical "1's"; hence, once again "0's" are put into the shift-register.

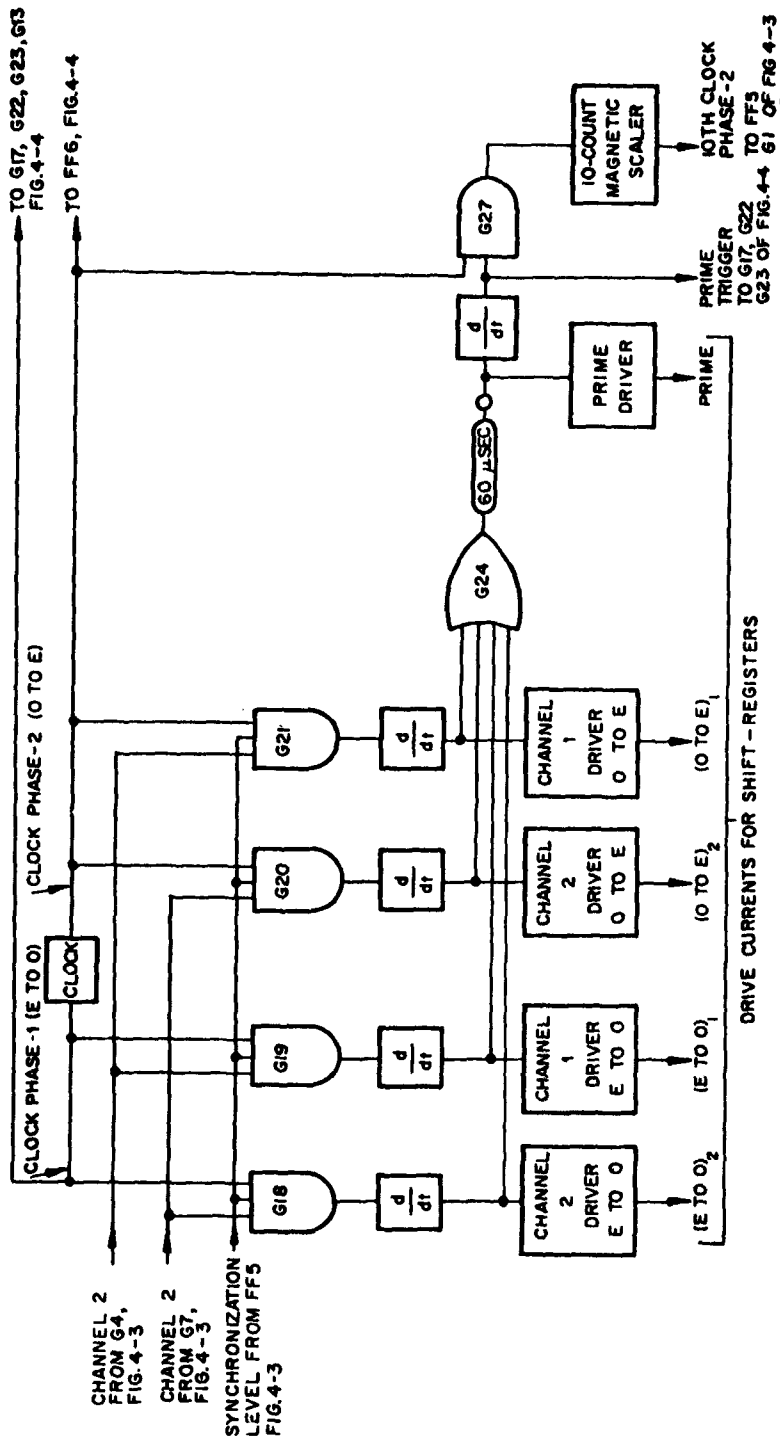


Fig. 4-6 Shift-Register Channel-Selector and 10-Count Magnetic-Scaler Logic Diagram

The fourth bit is the first "0" out of the shift-register and according to the algorithm should be converted to a "1." Since this bit is "0" (FALSE), FF6 remains reset. At prime-trigger clock phase-1, G22 is TRUE and FF7 is set. Gate G15 remains FALSE because the output from the shift-register is FALSE, but G16 is TRUE. The signal is then differentiated and channeled through G9 to trigger a blocking-oscillator which applies sets a "1" into shift-register channel 1. The differentiating gate now remains FALSE until after FF7 is set again. Flip-flop 7 provides a TRUE output only when the inputs change from FALSE to TRUE. This change cannot occur until the next input command because FF7 is not reset until after the tenth clock phase-2. Thus, at the fifth clock phase-1, only G15 reacts to the shift-register output since G17 and the differentiating gate G16 are FALSE. The fifth bit, being a "1," makes G15, G12, and G9 TRUE, resulting in a "1" being set into the shift-register. All succeeding bits are processed in the same manner, and the number in the shift-register after the tenth clock cycle is binary 0000011000 which is the required result.

The same logic is used for subtraction. The "add one" signal, being FALSE, inhibits G16 and G22. Flip-flop 7 was reset at the end of the last computation. As an example in describing the operation, assume that it is required to "subtract one" from binary 0000010110. The first bit out of the shift-register is a "0" and leaves FF6 in the reset state. Gate G15 is inhibited by FF7, and G23 remains FALSE since FF6 is reset. However, G17 is TRUE during phase-1 prime-trigger and causes a "1" to be set into the shift-register. The next bit is a "1" which sets FF6; this in turn inhibits G17 during clock phase-1. At prime-trigger clock phase-1, G23 is TRUE causing FF7 to be set. The net result of the above is to convert the second bit from a "1" to a "0." Thus, the setting of FF6 inhibits G17 during the second clock phase-1, and the setting of FF7 inhibits G17 from the second through the tenth clock phase-2. Thus, G15 allows the succeeding bits out of the shift-register to be reinserted unmodified. The clocking ceases after the tenth clock cycle; the number in the register is now 0000010101.

4.6 RESET LOGIC

The reset logic ensures that the system is cleared and properly indexed after the power has been turned on and prior to any input commands. This is accomplished by simulating an "add one" command to each channel and at the same time inhibiting G8 and G9. This places "0's" in every bit of both shift-registers. The output from the 10-count magnetic scaler is then used to set a "1" into a preselected bit in each shift-register.

Section 5
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